Technical Assistance Request:

Provide a two-page description of the unique challenges and needs a national lab, private facility, and/or member of the American-Made Network could potentially help you resolve. The Prize Administrator will make this request broadly available so members of the American-Made Network can understand your needs and assist you through the voucher program or otherwise.

In order to characterize and evaluate the medium voltage (MV) SiC MOSFETs, JBS diodes, and Hybrid-MOSFETs fabricated for this Solar Prize challenge, it will firstly be necessary to electrically test the devices on-wafer, and then subsequently electrically test the devices after packaging, in order to generate useful datasheets for partners and potential stakeholders to use when developing their next generation SST prototypes and products.

For the bare MV SiC device chips, forward conduction I-V curves, third-quadrant behavior (particularly body-diode and integrated JBS diode of the MOSFET and Hybrid-MOSFSET, respectively), transfer characteristics, threshold voltage, transconductance, gate charge, on-state resistance, capacitance (input, output, reverse transfer), and reverse blocking capability will need to be characterized at different voltages (up to 12 kV), currents (up to 50 A) and temperatures (up to 200C).

For the packaged MV SiC device chips, similar characterization will be required as performed for the bare MV SiC device chips, but will also include dynamic switching behavior in terms of turn-on, turn-off, and total switching energy at different gate-to-source voltages, drain-to-source, voltages, drain currents, cathode-to-anode voltages, anode currents, and temperatures in the ranges mentioned above.

Furthermore, for the packaged MV SiC device chips, it is of interest to evaluate the static reverse blocking behavior of the device when exposed to irradiation in order to evaluate the device for SST and other power electronics applications at high-altitude sites. This will aid in developing any necessary de-rating curves for the packaged MV SiC device chips.

Material analysis, in terms of SiC wafer material defects before and after various fabrication processes will also be beneficial in guiding raw material supplier selection, as well as understanding how original defects and/or defect growth/propagation might impact the overall project yield of producing the desired quantities of functional MV SiC devices.

Reliability testing is of recent interest to the SiC device community for both researchers and end-users in order to understand the expected mean life time to failure of new power electronic systems, such as the SST for PV, that look to take advantage of SiC devices. This will influence not only device design and architectures, but also safe-operating-area, de-rating safety margins, redundancy considerations for power systems,

etc. Having the ability to perform not only long-term high temperature testing such as high temperature gate bias (HTGB) and high temperature reverse bias (HTRB) in thermal chambers, thermal cycling and thermal shock tests of packaged MV SiC devices chips, and time dependent dielectric breakdown (TDDB) will help applications engineers better understand the capabilities and limitations of the devices in their systems. Having access to cross-section material examination using SEM / EDX would also be useful.

Lastly, any other power electronics circuits designers and applications engineers at national labs, universities, or US businesses that are interested in MV power semiconductor devices and/or SiC power semiconductor devices are welcome to perform their own evaluations of the MV SiC devices associated with this project. The more data points made available to us and the more feedback we can get from any potential end-user, the better the outcome technology will be and the greater chance SSTs for PV solar will be adopted sooner by major utilities around the country.